



2819 #6
8-22-2

Docket No. 174/211

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Chong Lee and Ramanand Venkata
Application No.: 10/059,014 Confirmation No.: 5565
Filed : January 29, 2002
For : CLOCK DATA RECOVERY WITH DOUBLE EDGE
CLOCKING BASED PHASE DETECTOR AND
SERIALIZER/DESERIALIZER
Group Art Unit : 2819

Hon. Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL LETTER FOR
INFORMATION DISCLOSURE STATEMENT

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Sir:

Transmitted herewith is an Information Disclosure Statement in the above-identified application. This Statement is submitted:

- ☒ [X] within three months of the application filing date;
☐ [] more than three months from the application filing date but before the mailing date of the first Office Action on the merits.

In accordance with 37 C.F.R. § 1.97, submission of this Statement requires no fee. However, if for any reason a fee is due, the Director is hereby authorized to charge payment of any fees required in connection with this

Information Disclosure Statement to Deposit Account

No. 06-1075. A duplicate copy of this letter is transmitted herewith.

Respectfully submitted,

Evelyn C. Mak

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INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97,
applicants wish to call the attention of the Examiner to the
following references:

U.S. PATENTS

3,473,160	Wahlstrom	10/14/69
5,689,195	Cliff et al.	11/18/97
5,909,126	Cliff et al.	06/01/99
6,215,326	Jefferson et al.	04/10/01

U.S. PATENT APPLICATION

09/516,921	Ngai et al.	03/02/00
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OTHER PUBLICATIONS

"Lucent Introduces 10Gb/s Ethernet FPGAs,"
Programmable Logic News and Views, November 2000
(Vol. IX, No. 11), pp. 7-8.

Protocol Independent Gigabit Backplane Transceiver
Using Lucent ORT4622/ORT8850 FPSCs, Application
Note, June 2000, Lucent Technologies Inc.,
pp. 1-10.

ORCA® ORT82G5 0.622/1.0 - 1.25/2.0 - 2.5/3.125
Gbits/s Backplane Interface FPSC, Product Brief,
February 2001, Lucent Technologies Inc., pp. 1-8.

ORCA® ORT82G5 1.0 - 1.25/2.0 - 2.5/3.125 Gbits/s
Backplane Interface FPSC, Preliminary Data Sheet,
July 2001, Agere Systems Inc., pp. 1-35.

ORCA® ORT8850 Field-Programmable System Chip (FPSC)
Eight-Channel x 850 Mbits/s Backplane Transceiver,
Product Brief, July 2001, Agere Systems Inc.,
pp. 1-6.

ORCA® ORT8850 Field-Programmable System Chip (FPSC)
Eight-Channel x 850 Mbits/s Backplane Transceiver,
Data Sheet, July 2001, Agere Systems Inc.,
pp. 1-36.

Rocket I/O™ Transceiver User Guide, v1.2,
(Feb. 25, 2002) <[http://www.xilinx.com/
publications/products/v2pro/userguide/ug024.pdf](http://www.xilinx.com/publications/products/v2pro/userguide/ug024.pdf)>.

Virtex-II Pro Platform FPGA Handbook, v1.0,
pp. 1-6, 27-32, 121-126, and 162-180,
(Jan. 31, 2002) <[http://www.xilinx.com/
publications/products/v2pro/handbook/ug012.pdf](http://www.xilinx.com/publications/products/v2pro/handbook/ug012.pdf)>.

Virtex-II Pro Platform FPGAs: The Platform for
Programmable Systems (visited 03/05/2002)
<<http://www.xilinx.com/virtex2pro>>.

These references are also listed on the attached
Form PTO-1449, and copies are enclosed.

Consideration of the foregoing in relation to this
patent application is respectfully requested.

Respectfully submitted,

Evelyn C. Mak

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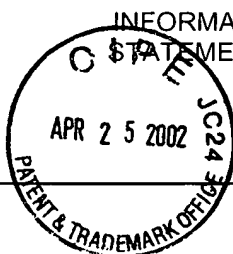
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FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
174/211APPLICATION
NO.
10/059,014INFORMATION DISCLOSURE
STATEMENT BY APPLICANTSAPPLICANTS
Chong Lee et al.CONFIRMATION
NO.
5565FILING DATE
January 29, 2002GROUP
2819

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	3,473,160	10.14.69	Wahlstrom			
	5,689,195	11.18.97	Cliff et al.	326	41	
	5,909,126	06.01.99	Cliff et al.	326	41	
	6,215,326	04.10.01	Jefferson et al.	326	41	
	U.S. Patent Appl. No. 09/516,921		Ngai et al.			03/02/00

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
	"Lucent Introduces 10Gb/s Ethernet FPGAs," <u>Programmable Logic News and Views</u> , November 2000 (Vol. IX, No. 11), pp. 7-8.
	Protocol Independent Gigabit Backplane Transceiver Using Lucent ORT4622/ORT8850 FPSCs, Application Note, June 2000, Lucent Technologies Inc., pp. 1-10.
	ORCA [®] ORT82G5 0.622/1.0 - 1.25/2.0 - 2.5/3.125 Gbits/s Backplane Interface FPSC, Product Brief, February 2001, Lucent Technologies Inc., pp. 1-8
	ORCA [®] ORT82G5 1.0 - 1.25/2.0 - 2.5/3.125 Gbits/s Backplane Interface FPSC, Preliminary Data Sheet, July 2001, Agere Systems Inc., pp. 1-35.
	ORCA [®] ORT8850 Field-Programmable System Chip (FPSC) Eight-Channel x 850 Mbits/s Backplane Transceiver, Product Brief, July 2001, Agere Systems Inc., pp. 1-6.
	ORCA [®] ORT8850 Field-Programmable System Chip (FPSC) Eight-Channel x 850 Mbits/s Backplane Transceiver, Data Sheet, July 2001, Agere Systems Inc., pp. 1-36.
	Rocket I/O [™] Transceiver User Guide, v1.2 (Feb. 25, 2002) < http://www.xilinx.com/publications/products/v2pro/userguide/ug024.pdf >.
	Virtex-II Pro Platform FPGA Handbook, v1.0, pp. 1-6, 27-32, 121-126, and 162-180 (Jan. 31, 2002) < http://www.xilinx.com/publications/products/v2pro/handbook/ug012.pdf >.
	Virtex-II Pro Platform FPGAs: The Platform for Programmable Systems (visited 03/05/2002) < http://www.xilinx.com/virtex2pro >.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.